REMARKS

Examiner G. Goudreau is thanked for the thorough examination and search of the subject Patent Application and for finding allowable subject matter in Claims 7, 16, and 17-20. Claims 9 and 17 have been amended and Claim 16 has been canceled.

All Claims are believed to be in condition for Allowance, and that is so requested.

Claim 9 has been amended in response to Examiner's objection to allowable Claim 16 as being dependent upon a rejected base Claim. Allowable Claim 16 has been incorporated into Claim 9.

Claim 17 has been amended to correct a typographical error in lines 9-10 and 13-14. Specifically, the original Claim 17, lines 9-10, referred to "providing a silicon dioxide layer overlying said silicon dioxide layer." The second reference to silicon dioxide in this section is incorrect. The step should have read, "providing a silicon dioxide layer overlying said silicon oxynitride layer." This usage is consistent with the drawings, the specification, and preceding Claims 7 and 16. Further, original lines 13-14 read, "patterning said resist layer to form a resist mask that exposes a

part of said silicon oxynitride layer." This time the reference to silicon oxynitride should have read "silicon dioxide" (the topmost layer). Therefore, lines 13-14 have been corrected to read, "patterning said resist layer to form a resist mask that exposes a part of said silicon dioxide layer." Once again, this is consistent with the drawings, the specification, and preceding Claims 7 and 16. Therefore, Claim 17 has been amended to correct these typographical errors and should remain in condition for allowance.

Reconsideration of Claims 1-6, rejected under 35 U.S.C. 103(a) as being unpatentable over Keller (U.S. Patent 5,346,586), in view of Hills et al (U.S. Patent 5,382,316), is requested based on the following remarks.

Applicant disagrees that the differences between Applicant and Keller, in view of Hills et al, are obvious to one skilled in the art. In particular, Applicant teaches a two-step process for stripping away the photoresist layer and then cleaning away any polymer residue. More specifically, Applicant first strips the photoresist layer using O_2 gas. Then, the polymer residue is removed using a chemistry containing CF_4 gas. In contrast, Keller, in view of Hills et al, as proposed by Examiner, uses a single step to remove the both the photoresist layer and the polymer sidewalls. Specifically, using the teachings of Hills et al, a single plasma

etch, comprising CF_4, H_2O, and O_2, is used to simultaneously remove the photoresist layer and the polymer sidewalls.

Applicant uses a photoresist stripping method (O_2 plasma) that allows for endpoint detection (see Specification page 16). Following this strip, the polymer clean step may be performed without endpoint detection. This polymer clean is critical for removing potential shorts from the semiconductor device surface. In addition, the etching chamber is pre-cleaned prior to the critical polysilicon etching step (see Specification pages 16-17).

The combination of the stripping and cleaning steps in Keller, in view of Hills et al, into a single step reflects a significant difference in approaches. Applicant's two step approach is a difference in approach with Keller, in view of Hills et al, that facilitates the above-mentioned endpoint detection and is not obvious to one skilled in the art. Therefore, Applicant believes that Claims 1-6 are in condition for allowance.

Reconsideration of Claims 1-6, rejected under 35 U.S.C. 103(a) as being unpatentable over Keller, in view of Hills et al is requested based on the above remarks.

Reconsideration of Claims 8-15, rejected under 35 U.S.C. 103(a) as being unpatentable over Keller, in view of Hills et al, and further in view of Chapman (US Patent 5,976,769), is requested based on Amended Claim 9 and on the following remarks.

It is agreed that Chapman discloses trimming of a resist mask. However, as discussed above, Applicant's two step approach to stripping the resist mask and then cleaning the polymer is a difference in approach with Keller, in view of Hills et al, that facilitates endpoint detection and is not obvious to one skilled in the art. Therefore, it is believed that the Claims are patentable over the references.

Furthermore, it is agreed with the Examiner that none of the references disclose a silicon dioxide layer overlying the hard mask layer and underlying the resist layer. This allowable material has been incorporated into Claim 9 from Claim 16.

Reconsideration of Claims 8-15, rejected under 35 U.S.C. 103(a) as being unpatentable over Keller, in view of Hills et al, and further in view of Chapman, is requested based on the Amendment to Claim 9 and on the above remarks.

Applicants have reviewed the prior art made of record and not relied upon, specifically, US Patent 6,130,166 to Yeh and US Patent 5,804,088 to McKee, and agree with the Examiner that while the references are of general interest, they do not apply to the detailed Claims of the present invention.

Allowance of all Claims is requested.

Attached hereto is a marked-up version of the changes made to the Claims by the current amendment. The attached pages are captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

It is requested that should Examiner G. Goudreau not find that the Claims are now Allowable that he call the undersigned at 765 4530866 to overcome any problems preventing allowance.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claim 9 has been amended as follows:

9. (Amended) A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a polysilicon layer overlying a semiconductor substrate;

providing a hard mask layer overlying said polysilicon layer;

providing a silicon dioxide layer overlying said hard mask layer;

providing a resist layer overlying said hard mask layer;

patterning said resist layer to form a resist mask that exposes a part of said hard mask layer;

patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said resist mask to trim said resist mask;

thereafter etching said hard mask layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said resist mask wherein said cleaning away comprises a chemistry containing CF_4 gas; and

thereafter etching said polysilicon layer exposed by said hard mask; and

stripping away said hard mask to complete the patterning of said polysilicon layer in the manufacture of the integrated circuit device.

Claim 17 has been amended as follows:

17. (Amended) A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a gate oxide layer overlying a semiconductor substrate;

providing a polysilicon layer overlying said gate oxide layer;

providing a silicon oxynitride layer overlying said polysilicon layer;

providing a silicon dioxide layer overlying said silicon [dioxide] <u>oxynitride</u> layer;

providing a resist layer overlying said silicon dioxide layer;

patterning said resist layer to form a resist mask that exposes a part of said silicon [oxynitride] dioxide layer;

patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said resist mask to trim said resist mask;

thereafter etching said silicon dioxide layer and said silicon oxynitride layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said resist mask wherein said cleaning away comprises a chemistry containing CF_4 gas; and

thereafter etching said polysilicon layer exposed by said hard mask wherein said etching comprises a main etch step followed by an overetch step; and

stripping away said hard mask to complete the patterning of said polysilicon layer in the manufacture of the integrated circuit device.